SILVER OAK UNIVERSITY

College of Technology
Master of Technology
Electronics and Communication
Course Name: Digital Design using HDL and FPGA
Course Code: 1010097102
Semester: 1st

Prerequisite:
Logic gates and flip-flops, Combinational and sequential Logic circuits

Course Objective:

1. This course is the first step for PG students in the ASIC prototyping field, also called FPGA (Field programmable gate array) / SoC (System on Chip) prototyping.

2. With large resource of configurable logic blocks FPGA is designed to be configured by designer using hardware description language for digital system design.

Teaching Scheme:

Teaching Scheme				
L	T	P	Contact Hours	Credit
3	0	2	5	4

Content:

Unit No.	Course Contents	Teaching Hours	Weightage %
1	**Introduction:** ASIC Design flow, Design Methodologies, Hardware modeling issues, Overview of FPGA and CPLD technology	3	10
2	**Hardware Description Language:** Elements of VHDL, Entity, architecture, configuration declaration. Identifiers, data types and operators, Assignment statement, Objects in VHDL – signals, variables, constants, files, Attributes of objects	6	10
3	**Behavioral modeling:** Process statement, Signal and variable assignment, Wait statement, if statement, Case statement, Loops, exit, and next statement, Assertion and report statement, Multiple process, Postponed process. Subprograms – procedures and functions, Subprogram overloading and operator overloading. RTL description	6	15

4	**Dataflow modeling:** Concurrent signal assignment, sequential signal assignment, delta delay, multiple drivers, conditional signal assignment using when if else, selected signal assignment using with select, block statement, concurrent assertion signal	6	15
5	**Structural modeling:** Component declaration, generics and component instantiation, Example of making hierarchical circuit. Generate statement, aliases, mixed modeling style Configuration and packages Configuration specification and declaration, conversion functions, direct instantiation, incremental binding. Package declaration, package body, design file	6	15
6	**Programmable Logic Design Basics of Programmable logic devices** - PROM, PAL, PLA, etc, CPLD architecture and its building blocks, FPGA architectures and its building blocks, Carry chains in FPGA, Dedicated multipliers and memory in FPGA, RTL synthesis test methodology, Design synthesis, Technology mapping for FPGAs: SRAM, Fuse, Antifuse, EPROM programming techniques. Design implementation using CPLD and FPGA, Floor planning, Placement and routing	8	25

Course Outcome:

Sr. No.	CO statement	Unit No
CO-1	Understand the basics of ASIC design and VHDL architecture	1,2
CO-2	Design digital system using different modeling style in VHDL	3,4,5
CO-3	To study use the Configuration and packages specification 7 declaration	6
CO-4	Design and understand how to write Test benches	7
CO-5	learn how to program and test programs on FPGAs or CPLD	8

Teaching & Learning Methodology:-

Projector, Slides

List of Experiments/Tutorials: **Total Hours: 28**

Sr. No.	Practical Name
1	Write entity with 2 inputs a, b and 7 outputs x1 to x7 for logic gates NOT, AND, OR, NAND, NOR, XOR, XNOR respectively
2	Write code for 4x1 MUX with structural modeling and using same, implement 8x1 MUX. Extend above programs for 16x1 MUX
3	Write code for 2x4 Decoder with structural modeling and using same, implement 3x8
	decoder. Extend program for 4x16 decoder.
4	Write code for D-latch with structural modeling and implement 4-bit register using same. Extend above program for 16-bit register
5	Write VHDL code to realize a 4 bit, 4 X 1 multiplexer.
6	Implement the following in VHDL code. • An 8-bit ripple adder (use equations)
7	To test VHDL code to implement various flip flops.
8	Test VHDL code to implement up counter.
9	Write VHDL code to implement down counter.
10	Test VHDL code for sequence detector using FSM

Major Equipment:

Kits with Xilinx / Altera FPGA

Books Recommended:-

1. J. Bhasker, VHDL Primer, Pearson Education Asia, Low Price Edition
2. Douglas L. Perry, VHDL programming by examples, 4th Ed., Tata McGraw Hill
3. Charles H Roth, Jr., Principles of Digital Systems Design using VHDL, Cengage Learning
4. Michael John Sebastian Smith, Application Specific Integrated Circuits, Pearson Education Asia

List of Open Source Software/learning website:

Xilinx ISE

CO-PO Matrix:

CO No.	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO 2
CO-1	3	2			2			2				2		3
CO-2	3	3	2	2					3			2	3	3
CO-3		3		2	2	2	2		3		2	2		-
CO-4	3	2	2			2		2	3			2		3
CO-5	3	2		2		2		2				2	2	3